Application No. 09/522,470 Amendment under 37 C.F.R. §1.114 Group Art Unit: 2193 Attorney Docket No.: 000267

AMENDMENTS TO THE CLAIMS

The below listing of claims replaces all prior versions of claims in the application.

**Listing of Claims:** 

1. (Currently Amended) A logic circuit, comprising:

a first inversion section for inverting a first input signal having a first logic level and

outputting an inverted first input signal;

a second inversion section for inverting a second input signal having a logic level <u>always</u>

being opposite to the first logic level, and outputting an inverted second input signal; and

a transmission section for receiving the inverted first input signal and the inverted second

input signal and outputting one of the inverted first input signal and the inverted second input

signal,

wherein the transmission section comprises electrically connected transistors that

respectively receive the inverted first input signal and the inverted second input signal, and the

connected transistors output one of the inverted first input signal and the inverted second input

signal in response to only an externally controllable selection signal and an inverted signal of the

selection signal.

2. (Currently Amended) A logic circuit, comprising:

a first inversion section for inverting a first input signal and outputting an inverted first

input signal;

- 2 -

Amendment under 37 C.F.R. §1.114 Attorney Docket No.: 000267

a second inversion section for inverting a second input signal which is always opposite to the first input signal, and outputting an inverted second input signal;

a first outputting section comprising electrically connected transistors for respectively receiving the inverted first input signal and the inverted second input signal, and the electrically connected transistors output one of the inverted first input signal and the inverted second outputinput signal in response to an externally controllable first selection signal and an inverted signal of the first selection signal; and

a second outputting section comprising electrically connected transistors for respectively receiving the inverted first input signal and the inverted second input signal, and the electrically connected transistors output one of the inverted first input signal and the inverted second input signal in response to only an externally controllable second selection signal and an inverted signal of the second selection signal.

## 3.-6. (Cancelled)

7. (Previously Presented) A logic circuit, comprising:

a first inversion section for inverting a first input signal and outputting the inverted signal;

a second inversion section for inverting the inverted signal of the first input signal and outputting a resulting signal;

Application No. 09/522,470 Amendment under 37 C.F.R. §1.114
Group Art Unit: 2193 Attorney Docket No.: 000267

a first outputting section for performing NANDing arithmetic between the output of said

first inversion section and a second input signal and outputting a first resulting signal; and

a second outputting section for performing NANDing arithmetic between the output of

said second inversion section and an inverted signal of the second input signal and outputting a

second resulting signal;

said first outputting section and said second outputting section being switched with the

second input signal and the inverted signal of the second input signal, said first outputting section

outputs the first resulting signal and said second outputting section outputs the second resulting

signal.

8. (Previously Presented) The logic circuit as claimed in claim 1, further comprising:

a first switching section provided on an input side of said first inversion section and

performing switching of whether the first input signal is passed to the first inversion section or

blocked in accordance with an external control signal; and

a second switching section provided on an input side of said second inversion section and

performing switching of whether the second input signal is passed to the second inversion section

or blocked in accordance with the external control signal.

9. – 12. (Cancelled)

- 4 -

Application No. 09/522,470

Group Art Unit: 2193

Amendment under 37 C.F.R. §1.114

Attorney Docket No.: 000267

13. (Currently Amended) A logic circuit, comprising:

a first inversion section for inverting a first input signal having positive logic and

negative logic and outputting an inverted first input signal, said first inversion section including

transistor circuits, each of said transistor circuits having a first input signal terminal for inputting

the first input signal and an outputting terminal for outputting the inverted signal based on the

logic of the first input signal;

a second inversion section for inverting a second input signal having negative logic and

positive logic always being opposite to the first input signal, said second inversion section

including transistor circuits, each of said transistor circuits having a second input signal terminal

for inputting the second input signal and an outputting terminal for outputting the inverted signal

based on the logic of the second input signal; and

a transmission section for selectively outputting one of the output of said first inversion

section and the output of said second inversion section in accordance with a logical value which

depends upon an externally controllable selection signal and an inverted signal of the selection

signal, said transmission section including transistor circuits, each of said transistor circuits

having a first selection signal terminal for inputting the controllable selection signal and a second

selection signal terminal for inputting the inverted signal of the selection signal.

14. (Cancelled)

- 5 -

Application No. 09/522,470

Group Art Unit: 2193

Amendment under 37 C.F.R. §1.114

Attorney Docket No.: 000267

15. (Currently Amended) A logic circuit, comprising:

a first inverter inverting a first input signal having a first logic level and outputting an

inverted first input signal;

a second inverter inverting a second input signal having a logic level always being

opposite to the first logic level and outputting an inverted second input signal; and

a selector to receive the inverted first input signal and the inverted second input signal

and to selectively output one of the inverted first input signal and the inverted second input

signal,

wherein the selector comprises electrically connected transistors that respectively receive

the inverted first input signal and the inverted second input signal, and the connected transistors

output one of the inverted first input signal and the inverted second input signal in response to

only an externally controllable selection signal and an inverted signal of the selection signal.

16. (Currently Amended) A logic circuit, comprising:

a first inversion section for inverting a first input signal having positive logic and

negative logic and outputting an inverted first input signal, said first inversion section including

Complementary Metal Oxide Semiconductor (CMOS) logic circuits, each of said CMOS logic

circuits having a first input signal terminal for inputting the first input signal, and an outputting

terminal for outputting the inverted signal based on the logic of the first input signal;

a second inversion section for inverting a second input signal having negative logic and

positive logicalways being opposite to the first input signal, said second inversion section

- 6 -

Amendment under 37 C.F.R. §1.114 Attorney Docket No.: 000267

Application No. 09/522,470

Group Art Unit: 2193

including CMOS logic circuits, each of said CMOS logic circuits having a second input signal

terminal for inputting the second input signal and an outputting terminal for outputting the

inverted signal based on the logic of the second input signal; and

a transmission section for selectively outputting one of the output of said first inversion

section and the output of said second inversion section in accordance with a logical value which

depends upon an externally controllable section signal and an inverted signal of the selection

signal, said transmission section including CMOS logic circuits, each of said CMOS logic

circuits having a first selection signal terminal for inputting the controllable selection signal and

a second selection signal terminal for inputting the inverted signal of the selection signal.

17. (Currently Amended) A logic circuit, comprising:

a first inversion section for inverting a first input signal with a first logic level and

outputting the inverted first input signal;

a second inversion section for inverting a second input signal with a second logic level,

which is always opposite to the first logic level, and outputting the inverted second input signal;

and

a transmission section for receiving the inverted first input signal and the inverted second

input signal and outputting either the inverted first input signal or the inverted second input

signal.

- 7 -

Amendment under 37 C.F.R. §1.114 Attorney Docket No.: 000267

Application No. 09/522,470

Group Art Unit: 2193

18. (Previously Presented) The logic circuit as claimed in claim 17, further comprising:

a first switching section provided on an input side of said first inversion section and

performing switching of whether the first input signal is passed to the first inversion section or

blocked in accordance with an external control signal; and

a second switching section provided on an input side of said second inversion section and

performing switching of whether the second input signal is passed to the second inversion section

or blocked in accordance with the external control signal.

- 8 -